REASONS FOR ALLOWANCE

Terminal Disclaimer

The terminal disclaimer filed on 12/16/09 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,592,690 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowance

Claims 34-37, 46, 53-58 and 60 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 34, the prior art of record is neither anticipated nor rendered obvious all the limitations including the chip size packaged type semiconductor device having a second semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface, wherein the back surface and the entirety of the side surfaces of the second semiconductor element are exposed, wherein the chip size packaged type semiconductor device has a second resin that covers the main surface of the second semiconductor element and side surfaces of the terminals, the first and second resins that are separate from each other, and wherein a gap without resin exists between the second semiconductor element and the backside surface of the base plate.

Regarding claim 53, the prior art of record is neither anticipated nor rendered obvious all the limitations including the chip size packaged type semiconductor device having a second semiconductor element which has main and back surfaces, and side

surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface, wherein the back surface and the entirety of the side surfaces of the second semiconductor element are exposed, wherein the main surface of the second semiconductor element is sealed with a second resin, and portions of each of the plurality of terminals are exposed from the second resin, the first and second resins are separate from each other, wherein a gap without resin exists between the second semiconductor element and the backside surface of the base plate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH P. NGUYEN whose telephone number is (571) 272-1712. The examiner can normally be reached on 9:00 AM - 6:30 PM (Monday-Thursday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

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/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893